

**A 4-bit Controlled Buffer Register**

**module cbr (CK, DIN, Q, LD, CLR);**

**input CK, LD, CLR;**

**input [7:0] DIN;**

**output [7:0] Q;**

**reg [7:0] Q;**

**always @(negedge CK)**

**if (~CLR)**

**Q = 8'h00;**

**else**

**if (LD)**

**Q = DIN;**

**endmodule**

**module test\_cbr;**

**reg CK, LD, CLR;**

**reg [7:0] DIN;**

**wire [7:0] Q;**

**cbr r1 (CK, DIN, Q, LD, CLR);**

**always**

**#3 CK = ~CK;**

**initial**

**begin**

**CK = 0;**

**DIN = 8'b10101010;**

**#20 DIN = 8'hFF;**

**#5 DIN = 8'hAB;**

**end**

**initial**

**begin**

**LD = 0;**

**CLR = 0;**

**#10 LD = 1;**

**#5 CLR = 1;**

**#12 LD = 0;**

**end**

**endmodule**